AF/IFW

Attorney Docket 944-003.225

IN THE U.S. PATENT AND TRADEMARK OFFICE

Re application of :

Matti Floman, et al :

Serial No. 10/817,448 : Examiner: Duc T. Doan

Filed: April 2, 2004 : Group Art Unit: 2188

For: A FAST NON-VOLATILE RANDOM ACCESS MEMORY IN ELECTRONIC DEVICES

REPLY BRIEF

Director
U.S. Patent & Trademark Office
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Examiner's Answer of March 5, 2008, Applicant responds as follows:

***If any fee and/or extension is required in addition to any enclosed herewith, please charge Account No. 23-0442.**

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is, on the date shown below, being:

MAILING

☒ Deposited with the United States Postal Service with sufficient postage as first class Mail in an envelope addressed to the Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450.

FACSIMILE

☐ Transmitted by facsimile to the U.S. Patent and Trademark Office.

Date: April 9, 2008

Jennifer Hanlon
Signature
Jennifer Hanlon
(type or print name of person certifying)

REMARKS

This Reply Brief is in response to the the Examiner's Answer of March 5, 2008 in which rejection of all claims under appeal was confirmed.

***

Upon further review of references quoted by the Examiner, the applicant has come to the conclusion that **Lin does not disclose double data interface** configured to provide communication with the processor (e.g., between the processor and the fast NVRAM), as recited in independent claims 1, 20 and 33 (further clarification is provided in claim 2) of the present invention, contrary to what is alleged by the Examiner. Lin **does not** disclose **double data interface** but simply mentions that "DRAM 68, such as a double data rate (DDR), memory is **used for storing data and programs**." (see col. 4, lines 38-40 of Lin). Nothing in Lin indicates or even hints that the interface between the processor 62 and a north bridge circuit 64 (which can be equivalent to the ASIC 28 in figure 1a, 2a or 2b of the present invention) uses a double data rate, as recited and disclosed in the present invention. In other words, the goal of Lin is to make sure that the **memory 68 has enough capacity** when a hard disk drive is substituted by the memory 68 (see title and ABSTRACT of Lin), and the data compressing/decompressing module 78 (part of the module 64 of Lin) "**is used for compressing data that is about to be stored to reduce the corresponding data size in the DRAM (68) and decompressing compressed data retrieved from the DRAM (68) during the recovery of the original data.**" (see col. 4, lines 51-56 of Lin). Thus double data rate is used by Lin only for storing the data in the memory 68 and not for communicating

with the processor (i.e., CPU 62 of Lin), contrary to what is recited, claimed and disclosed in the present invention.

Summarizing, none of the references quoted by the Examiner, disclose **double data interface configured to communicate with the processor**, as recited in independent claims 1, 20 and 33 of the present invention. Therefore, based on the above arguments, claims 1, 20 and 33 (and consequently their dependent claims) of the present invention are not obvious under 35 U.S.C. 103(a) as being unpatentable over Ganton in view of Lin and in further view of Eaton et al, because references quoted by the Examiner must teach or suggest **all the claim limitations** per MPEP Paragraph 2143.

***

In the Examiner's Response to the Appeal Brief, he primarily presented the same or similar arguments to justify combining **multiple references** (at least three at a time) in the hindsight to arrive at the subject matter of the claims of the present invention. Following the Examiner's logic, any invention in the past or in the future can be found obvious by arbitrarily combining different aspects of the inventions known from different sources.

One question which is repeatedly raised by the Examiner is the definition of **fast non-volatile RAM (fast NVRAM)** which is used in the claims of the present invention. The Examiner argued that the **NVRAM** could be a volatile memory backed by a battery and demonstrated some definitions in that regard.

Unfortunately, NVRAM is not an exactly defined term, but has in the past sometimes referred to a battery backed SRAM or DRAM, or in some other cases "shadowed" (S)RAM + EEPROM, where the data is copied from RAM to EEPROM during power down, and externally the component looks like one memory (i.e. SRAM).

However, recently NVRAM has been often used with new, non-conventional memory technologies such as FeRAM, MRAM and Phase Change RAM or comparable technologies which are non-volatile, read like RAM and write/program like RAM or at least significantly faster than traditional NVM, like Flash or EEPROM. The specification of the present invention on page 11, lines 3-6 refers to these new technologies as follows: "According to the present invention, the fast NVRAM **16** can be, for example, a magneto-resistive random access memory (MRAM), a ferroelectric random access memory (FeRAM), an Ovonics type memory or any other type of emerging technologies" which do not require battery backup. Then non-volatile memory types (which do not require battery backup) mentioned above are prime candidates to be used in the context of embodiments of the present invention.

Then if we assume for the sake of argument only that **only non-volatile memory types without memory backup** are intended by the present invention, then combining references of Ganton and Lin is incompatible (i.e., teaching away from the present invention recited, e.g., in claim 1 and other independent claims) because Lin discloses only non-volatile memory with the battery backup. However, even without this assumption, there is enough evidence in the Appeal Brief to show a problematic nature of establishing *prima facie* case of obviousness by the USPTO.

First, not all limitations recited in the independent claims 1, 20 and 33 of the present invention are taught by the references quoted by the Examiner as articulated herein (e.g., double data interface for communicating with the processor is not disclosed by Lin or other references quoted by the Examiner).

Moreover, even if we assume **for the sake of argument only** that all limitations of independent claims 1, 20 and 22 are disclosed by the references quoted by the Examiner, in principle

we can use battery backup in a portable electronic device which normally uses a battery anyway, as pointed out by the Examiner. However, this will draw additional battery power needed for other purposes in the portable device (e.g., camera/phone). Therefore, the applicant is of opinion that from the practical point of view using battery backed-up memory in a portable device would not make sense when other fast "non-battery non-volatile" alternatives (see page 11, lines 3-6 of the present patent application) are available. For that reason, incorporating Lin into Ganton would not make sense (i.e., will not provide a motivation for a person skilled in the art to do so), contrary to what is alleged by the Examiner.

As far as motivation to combine references and problem to be solved, the Examiner's arguments are not convincing to the applicant. As was pointed out herein, Lin's goal is not to provide a fast interface with the processor 62, but to store as much data as possible in the memory 68 9an alternative to the hard disk drive), contrary to what is alleged by the Examiner. This makes Examiner's arguments even more problematic.

As far as dependent claims, practically, the Examiner did not present any new evidence and did not present convincing arguments to account for unique limitations of the dependent claims and/or to provide motivation/rationale for combining multiple references in order to demonstrate *prima facie* case of obviousness. Examiner's arguments in regard to unique limitations of claims 5 and 7 and other dependent claims continue to be incomplete and inaccurate ignoring or misinterpreting argument presented by the Applicant in the Appeal brief.

***

The objections and rejections of the Examiner's Answer to the Appeal Brief having been obviated by a **new evidence** in

regards to the double-data interface and other presented arguments, withdrawal thereof is requested and passage of claims under Appeal to issue is solicited.

Respectfully submitted,

A. Frenkel

Date: April 9, 2008

Anatoly Frenkel
Registration No. 54,106

WARE, FRESSOLA, VAN DER SLUYS
& ADOLPHSON LLP
755 Main Street, PO Box 224
Monroe CT 06468
(203) 261-1234